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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,765	09/10/2003	Yukiya Hirabayashi	116801	4078

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
SCHECHTER, ANDREW M	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,765	HIRABAYASHI, YUKIYA	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 June 2005 has been entered.

Response to Arguments

2. Applicant's arguments filed 28 June 2005 have been fully considered but they are not persuasive.

The applicant argues that *Sawatsubashi* does not disclose the limitations amended to claims 1, 2, and 6. This is not persuasive, as discussed below.

Claim Objections

3. Claim 2 is objected to because of the following informalities: in line 7, "a counter comprising" should be "a counter substrate comprising". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.,* U.S. Patent No. 5,148,301 in view of *Shirahashi et al.,* U.S. Patent No. 5,285,301.

Sawatsubashi discloses [see Figs. 3-5] an electro-optical device comprising an active matrix substrate [101] having on the same plane a plurality of scanning lines [G1-Gm], a plurality of signal lines [D1-Dn] provided to intersect the scanning lines, a plurality of pixel electrodes [103] provided at the intersection portions of the scanning and signal lines, and a peripheral driving circuit [112, 113] to matrix drive the pixel electrodes, the peripheral driving circuit including thin film transistors [col. 4, lines 58-62] each having a channel region [a channel region is an inherent part of a TFT, part of the semiconductor mentioned in the previous citation]; a counter substrate [102] having a common electrode [105] facing the pixel electrodes; a seal [108] that forms a sealed region between the substrate, with the peripheral driving circuit being disposed at least partially within the sealed region [see Figs. 3 and 4, and col. 4, lines 62-66]; a liquid crystal layer [109] disposed in the sealed region between the active matrix substrate and the counter substrate; wherein the common electrode is in a non-overlapping

arrangement with at least one of the peripheral driving circuit and wiring lines [114] for supplying signals to the peripheral driving circuit in plan view.

Sawatsubashi does not explicitly disclose a light shielding film on the counter substrate which is in a non-overlapping arrangement with at least one of the peripheral driving circuit and wiring lines. *Shirahashi* discloses [see Fig. 15, for instance] a light shielding film [BM] on the counter substrate which is in a non-overlapping arrangement with at least one of the peripheral driving circuit and wiring lines [the black matrix covers only the dummy pixel regions and the non-display areas of the pixels]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a black matrix in the device of *Sawatsubashi*, motivated by the teaching of *Shirahashi* that it protects the semiconductor layers and clarifies the contour of each pixel to improve the contrast [col. 9, lines 9-45]. Claim 1 is therefore unpatentable.

Sawatsubashi's peripheral driving circuit comprises a data line driving circuit [112], and the wiring lines comprise clock signal lines and image signal lines [col. 5, lines 33-38], so claim 5 is also unpatentable. It is an electronic apparatus, so claim 7 is also unpatentable.

Considering claim 6: as discussed above, *Sawatsubashi* in view of *Shirahashi* discloses a method of manufacturing an electro-optical device, comprising forming a plurality of pixel electrodes [103] and a peripheral driving circuit [112, 113] to matrix drive the plurality of pixel electrodes on one surface of an active matrix substrate [101], the peripheral driving circuit including TFTs each having a channel region; forming a common electrode [105] and light shielding film on one surface of a counter substrate

[102] and arranging them in a non-overlapping arrangement with at least one of the peripheral driving circuit and the wiring lines [114] for supplying signals to the peripheral driving circuit in plan view; bonding the active matrix substrate to the counter substrate with a predetermined gap using a sealing material [108] to form a sealed region, the peripheral driving circuit being disposed partially within the sealed region, and the common electrode facing the pixel electrodes; and forming a liquid crystal layer by injecting liquid crystal into the sealed region formed by the active matrix substrate, the counter substrate, and the sealing material [col. 4, lines 40-42]. Claim 6 is therefore unpatentable as well.

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.,* U.S. Patent No. 5,148,301 in view of *Shirahashi et al.,* U.S. Patent No. 5,285,301, as applied to claim 1 above, and further in view of *Yamamoto et al.,* U.S. Patent No. 5,506,705.

Sawatsubashi does not disclose single crystal silicon TFTs or driving signals to the peripheral driving circuit at a frequency equal to or more than 10 MHz. For an analogous LCD, *Yamamoto* discloses using single crystal silicon TFTs and a driving signal of 10 MHz [col. 12, lines 1-25]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use single crystal silicon TFTs and a 10 MHz driving frequency in the device of *Sawatsubashi*, motivated by *Yamamoto's* teaching that this allows high speed driving and thus improves the display quality. Claims 3 and 4 are therefore unpatentable.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.*, U.S. Patent No. 5,148,301 in view of *Ino,* US 2003/0112403.

Sawatsubashi discloses [see Fig. 11, a different embodiment than that relied on in the above rejection of claim 1] an electro-optical device comprising an active matrix substrate having on the same plane a plurality of scanning lines, signal lines, and pixel electrodes [103], and a peripheral driving circuit [113] to matrix drive the pixel electrodes including TFTs [col. 4, lines 58-62] with a channel region [inherent, as discussed above], and a counter substrate comprising a common electrode [105] facing the pixel electrodes and a light shielding film [124]; a seal [108], the peripheral driving circuit being disposed at least partially within the sealed region [see Fig. 11], and a liquid crystal layer [109] disposed in the sealed portion between the substrates.

Sawatsubashi does not explicitly disclose that the counter substrate and light shielding film are in a non-overlapping arrangement with the wiring lines for supplying signals to the peripheral driving circuit in plan view. (Since the peripheral driving circuit is at least partially within the sealed region between the substrates, it is at least partially between the substrates, so it must overlap the counter substrate; thus claim 2 can only be satisfied by having the counter substrate non-overlapping with the wiring lines supplying signals to the peripheral driving circuit.) *Ino* discloses an analogous LCD, with peripheral driving circuit [13] partially within the sealed region, like *Sawatsubashi's* circuit [113], and also discloses the peripheral driving circuitry including an IC chip [65] and external wiring [not labeled, but the equivalent of 611 on the left side of the chip in Fig. 6] supplying signals to the peripheral driving circuit. It would have been obvious to

one of ordinary skill in the art at the time of the invention to use such an IC chip and external wiring, motivated by *Ino's* teaching that by mounting such IC chips directly on the substrate, the portions electrically connected to the external circuits of the LCD panel can be reduced, so mechanical reliability is improved and defects in electrical connection are reduced [paragraph 0048]. In such case, the counter substrate and light shielding film would be in non-overlapping arrangement with the wiring lines for supplying signals to the peripheral driving circuit (that is, the wiring lines leading to the IC chip), so claim 2 is unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Schechter
Primary Examiner
Technology Center 2800
s12 September 2005